Atty Dckt Number: 2102397-911600

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Geeng-Chuan Chern

Application No. 09/916,618

Filed: July 26, 2001

For: SEMICONDUCTOR MEMORY ARRAY OF FLOATING GATE MEMORY CELLS WITH VERTICAL CONTROL GATE SIDEWALLS AND INSULATION SPACERS (as amended)

Group Art Unit: 2814

Examiner: Howard Weiss

RESPONSE TO FINAL OFFICE ACTION MAILED DECEMBER 11, 2002

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Box, Assistant Commissioner for Patents, Washington, DC 20231, on January 29, 2003.

GRAY CARY WARE & FREIDENRICH Date: 01/29/03

By: Kathleen LaBrie
Kathleen LaBrie

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Final Office Action mailed on December 11, 2002, please amend the above identified application as follows:

I. CLEAN VERSION OF CLAIMS AMENDED

Please substitute the following claim for the corresponding pending claim in this application:

1 ~~23~~. (Twice Amended) An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart regions in the substrate of a second conductivity type, with a channel region therebetween;

a first insulation layer disposed over said substrate;